Remarks

In the Office Action dated June 19, 2003 (hereinafter, "Office Action"), Claims 1-7 and 21-46 were rejected. The Claims remain as previously presented. In view of the arguments set forth below, it is submitted that the Claims are in condition for allowance as presently presented and an early Notice of Allowance is respectfully requested.

1. In the Office Action, Claims 22, 23, 28, 29, 33, 34, 38 and 45 were rejected under 35 USC §112 first paragraph for failing to comply with the written description requirement. These Claims are considered in turn as follows:

a.) Claim 22 describes instruction address generate logic to predict which instructions are to enter the fetch stages. This logic is discussed in reference to Applicants' Figures 7 and 10 as follows:

> "The IP of the preferred embodiment includes an Instruction Address Generate Section 111 that provides logic that generates an absolute instruction address by adding a relative address to the address of a designated base register within the IP. The absolute instruction address is provided to a tag memory (not shown in Figure 7) to determine if the addressed instruction is located in the I-FLC 38. If the instruction is resident in the I-FLC, the address is provided on Line 112 to the I-FLC so the addressed instruction may be retrieved and provided on Line 114 to the Instruction Queue Logic 116. (Specification page 16 lines 9-15 in reference to Figure 7.)

This aspect is further described in more detail in reference to Figure 10 as follows:

> "As discussed previously, Instruction Address Generation Section 111 generates an address that is provided to the I-FLC 38 to obtain the next instruction to execute. The actual address generation is performed by Instruction Address Generate Logic 200. This logic includes circuits to predict which sequence of instructions, and which instruction in particular, will be executed next. The predicted address is latched into Storage Device 202 at time 1Y1. This predicted address is provided to the Instruction Translation Look-ahead Buffer (TLB) 204 to determine if the address is likely stored in cache. The Instruction TLB stores a list of all pages of the Main Memory 46 that

> have been stored in the I-FLC 38, wherein each page of memory includes a predetermined number of addressable memory locations. In the preferred embodiment, each page of memory is 32K bytes in length." (Specification page 20 line 23 – page 21 line 4.)

It is respectfully submitted that these passages describe the claimed address generate logic. If this rejection is being made on the basis that Claim 22 fails to describe a specific algorithm used by the instruction address generate logic, it may be noted that many such algorithms are known in the art. (See, for example, U.S. Patent No. 5,611,065 to Alferness et al. entitled "Address Prediction for Relative-to-Absolute Addressing" assigned to Unisys Corporation.) The subject invention is related to decoupling of pipeline stages, and the aspects of the system that are already known to those skilled in the art, such as the workings of the instruction first-level-cache, instruction look-ahead buffer, and address generate logic, are not described in detail. If this rejection is not withdrawn, further clarification regarding this rejection is respectfully requested.

b.) Claim 23 claims instruction address generate logic that includes a circuit to clear ones of the fetch stages in response to a determination that instruction execution was re-directed. This is discussed in the Specification as follows:

> "According to still another scenario, it may be determined that the instructions resident in the pipeline must be flushed. This could occur, for example, because an unexpected re-direction occurred within the executing sequence of instructions as may be caused by the execution of a "JUMP" instruction. In such situations, all instructions that were previously fetched from memory for execution must be discarded and a different sequence of instructions retrieved for execution. The pipeline is flushed when the Instruction Address Generation Section 111 asserts the flush signal on Line 248, which allows a newly fetched instruction on Line 236 to enter stage 2Y as soon as the instruction becomes available. The assertion of this signal results in all pipeline storage devices including Storage Devices 240 and 250 of Figure 11 to discard any previously-stored instructions." (Specification page 23 lines 13-21 in reference to Figure 11.)

A description of a clearing of a pipeline stage during activation of the flush signal appears as follows:

> "When an instruction advances from stage 2Y to 3Y, it must also be selected by Select Circuit 266. Select Circuit selects the instruction on Line 268 when a flush operation is not occurring, as controlled by the de-activation of the flush signal on Line 248. When a flush operation is occurring, Select Circuit instead selects the "tied-low" inactive signals on the alternative input so that Storage Device 250 is effectively cleared. This prevents any inadvertent and undesired decode sequences from being initiated on Line 122 by Decode Logic 260 during the pipeline flush operation." (Specification page 24 line 24 – page 25 line 2.)

To summarize, the Instruction Address Generation Section 111 asserts a flush signal shown in Figures 7 and 11. This signal is asserted when certain instructions associated with address re-direction are detected. This signal is provided on line 248 to clear fetch pipeline stages shown in Applicants' Figure 11.

In view of the foregoing, it is believed this aspect of Applicants' invention is described and shown in a manner that satisfies the requirements of 35 USC § 112, first paragraph, and it is respectfully requested that this rejection be withdrawn.

c.) Claims 28 and 33 describe the address generate logic and flush aspect of Applicants' invention discussed above in regards to Claim 22. These Claims are believed to satisfy the requirements of 35 USC § 112 for the reasons discussed above in reference to Claim 22, and it is respectfully requested that these rejections be withdrawn.

d.) Claims 29 and 34 describe the aspect of Applicants' invention wherein stages of the pipeline are cleared by the address generate logic. These Claims are believed to satisfy the requirements of 35 USC § 112 for the reasons discussed above in reference to Claim 23, and it is respectfully requested that these rejections be withdrawn.

e.) Claim 38 describes the aspect of Applicants' invention wherein one of the fetch stages includes a circuit to allow retrieval of an instruction from either the memory or from the queue. This is discussed in Applicants' Specification in reference to Figure 11 as follows:

> "Upon being provided to Instruction Queue Logic 116, the instruction is stored in Storage Device 216 at time 2Y1. This instruction will either be provided to the Instruction Queue 218 storage device on Line 219, or will be provided on Line 220 directly to the Select Circuit 222 as will be discussed below. Instruction Queue stores up to a predetermined maximum number of instructions that have been retrieved from the I-FLC or other system memory and that are waiting to enter the 2Y and 3Y stages of instruction processing." (Specification page 21 lines 17 through 23.)

And as follows:

> "As mentioned previously, an instruction is only stored in Instruction Queue if other instructions are also stored in the Instruction Queue waiting to enter the 2Y stage of execution. Otherwise, if the Instruction Queue is empty, the instruction is provided directly on Line 220 to Select Circuit 222, and is forwarded to the 2Y/3Y Pipeline Logic 234. This allows an instruction to enter stage 2Y immediately after being read from the I-FLC if no other instructions are pending in the Instruction Queue. Selection control for Select Circuit 222 is provided by Queue Control Logic 232 on Line 235." (Specification page 22 lines 9 through 16.)

To summarize, if Instruction Queue 218 is empty, an instruction may be provided directly on line 220 from the instruction first-level cache (a memory) to the 2Y stage of the pipeline. Otherwise, the instruction is provided to the instruction queue for later entry into the 2Y stage. This functionality is provided by select circuit 222, queue control logic 232, and circuitry shown in Figure 10. Thus, this aspect of Applicants' invention is clearly shown in Applicants' Figures and described in the Specification in accordance with 35 USC § 112, and it is respectfully requested that this rejection be withdrawn.

f.) Claim 45 describes the aspect of Applicants' invention wherein an indication is provided that an operation occurring within the execution stages, and in response thereto, instructions are allowed to advance within the fetch stages. This is described in Applicants' Specification with respect to the dispatch function as follows:

> According to another aspect of the invention, the current pipeline system includes instruction flow control logic that allows instructions to advance within the fetch stages of the pipeline whenever a predetermined logic section within the execution pipeline stages is performing a predetermined function. In the preferred embodiment, instructions are allowed to advance within the fetch

> stages of the pipeline whenever the dispatch logic section included within the execution stages of the pipeline is performing a dispatch function. Whenever a dispatch function is completed, instructions are allowed to advance within the execution stages of the pipeline at a next predetermined time interval as dictated by the system clock. This allows the execution stages of the pipeline to accept another instruction for processing. Therefore, the occurrence of the dispatch function indicates that instructions may also advance within the fetch stages of the pipeline. (Applicants' Specification page 8 line 27 – page 9 line 8.)

This is further described as follows:

> According to another scenario, the instruction on Line 236 is selected for storage in Storage Device 240 if an instruction completes stage 1X, or is "dispatched". This is indicated by the assertion of the instruction dispatch signal on Line 246, as is provided by the Instruction Decode Dispatch Logic 124. An instruction is latched into the Storage Device 240 in this situation because the dispatch of an instruction will cause all instructions resident in stages 1X through 6X to advance so that the execution stages of the pipeline can accept another instruction. As a result, all instructions within the fetch stages 0Y through 3Y of the instruction pipeline also may advance. (Applicants' Specification page 23 lines 6 –12 in reference to Figures 7 and 11.)

Thus, it is believed that the aspect of Applicants' invention claimed by Claim 45 is described in Applicants' Specification and depicted within the drawings in a manner that satisfies the requirements of 35 USC § 112 first paragraph, and it is respectfully requested that this rejection be withdrawn.

In summary, it is submitted the various aspects of the invention claimed by Applicants' Claims 22, 23, 28, 29, 33, 34, 38 and 45 are clearly and concisely described in the Specification and depicted in the drawings in a manner that conveys to one skilled in the relevant art that the inventor(s) had possession of the claimed invention at the time the application was filed. It is therefore requested that this rejection be withdrawn.

2. Claims 1, 21, 27, 32, 39, 40 and 46 are rejected under 35 USC 103(a) as being unpatentable over U.S. patent no 6,112, 295 to Bhamidipati et al. (hereinafter "Bhamidipati") in view of Hayes, John P., "Computer Architecture and Organization", (hereinafter "Hayes"). This rejection is respectfully traversed.